



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/828,492

04/21/2004

Sadami Takeoka

60188-820

5291

7590

06/07/2006

McDermott, Will & Emery  
600 13th Street, N.W.  
Washington, DC 20005-3096

EXAMINER

DICKEY, THOMAS L

ART UNIT

PAPER NUMBER

2826

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/828,492

Applicant(s)

TAKEOKA ET AL.

Examiner

Thomas L. Dickey

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 09 May 2006.  
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 11-18 is/are pending in the application.  
4a) Of the above claim(s) 17 and 18 is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 11,12,14 and 15 is/are rejected.  
7) ☒ Claim(s) 13 and 16 is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 21 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☒ Certified copies of the priority documents have been received in Application No. 10/187,269.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 8/11/04.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_

Art Unit: 2826

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/9/06 has been entered.

### ***Information Disclosure Statement***

2. The Information Disclosure Statement filed on August 11, 2004 has been considered.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 11, 12, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over JARWALA ET AL. (5,673,276) in view of KOMOIKE (6,094,736).

Art Unit: 2826

With regard to claims 11 and 12 Jarwala et al. disclose a semiconductor device comprising a semiconductor wiring substrate 10, said semiconductor wiring substrate 10 being composed of a ceramic, having a wiring ("leads," not shown for the sake of clarity, note column 3 line 53) layer; a plurality of chip IPs 14 mounted on said semiconductor wiring substrate 10 by being bonded thereto; a boundary scan test circuit 16 provided in each of said chip IPs 14; and scanning signal input terminals 53' and 53 connected to an internal scan chain (note column 5 lines 62-65), at least one of said scanning signal input terminals 53' and 53 being a terminal 53 specially formed separately from said boundary scan test circuit 16; wherein said internal scan chain is for an internal scan test (such as described at column 4 lines 36-47) provided in each of said chip IPs 14, and the boundary scan test circuit 16 and the internal scan chain for an internal scan test are formed so as to be capable of performing respective scan tests simultaneously with each other, using test data which is input from outside. Note figures 3-6 and 9-12 of Jarwala et al.

Jarwala et al. do not disclose that said ceramic is semiconductor material. However, Komoike discloses a semiconductor wiring substrate 1 being composed of a semiconductor (note figure 1) on which a plurality of semiconductor chip IPs 2,4 are to be mounted; and a plurality of pieces of wiring 7 formed on the semiconductor substrate 1 to be used only for testing. Note figure 1 of Komoike. Why should one substitute the semiconductor substrate of Komoike for the ceramic substrate of Jarwala et al.? One having skill in the Multi-chip Module Art would know. A mismatch in the materials used for the substrate and the chips bonded thereon could result in a TCE (thermal

Art Unit: 2826

coefficient of expansion) mismatch. When the assembly is heated, the substrate and chips could expand at different rates, resulting in potentially damaging stress between the constituent parts. This problem is often discussed in the art, for example at column 1 lines 17-40 of Canestaro et al. 4,728,751. Therefore, it would have been obvious to a person having skill in the art to replace the ceramic material of Jarwala et al.'s substrate with the semiconductor material such as taught by Komoike in order to match the material, and thus the CTE, of the chip IPs to thus avoid possible damage due to thermal stress.

With regard to claims 14 and 15 Jarwala et al. disclose a semiconductor device comprising a semiconductor wiring substrate 10, said semiconductor wiring substrate 10 being composed of a semiconductor material, having a wiring ("leads," not shown for the sake of clarity, note column 3 line 53) layer; a plurality of chip IPs 14 mounted on said semiconductor wiring substrate 10 by being bonded thereto; a boundary scan test circuit 16 provided in each of said chip IPs 14; and at least two pieces of wiring (leads are not shown for the sake of clarity, note column 3 line 53, the "external" wiring is shown in the circuit diagram of figures 9 and 10 as part #56) for inputting (note column 8 line 30) test data from outside or outputting a test result directly to outside (again note column 8 line 30, also note the preamble to claim 1) from said boundary scan test circuit 16 of at least one of said chip IPs 14; said at least two pieces of wiring being formed in the wiring layer of said semiconductor wiring substrate 10; and an input terminal (TDI 18) and an output terminal (TDO 34) for a boundary scan test (such as described at column 4 lines 36-47) connected to said boundary scan test circuit 16 in each of said

Art Unit: 2826

chip IP 14 and respectively connected to said two pieces of wiring for testing only, wherein said boundary scan test circuit 16 in said plurality of chip IPs 14 is formed so as to also function as an internal scan test circuit 16 in said chip IPs 14 wherein, in each (note figure 4, showing the circuit 16 of chip 14) of said chip IPs 14, an input-side wiring branch TDI and an output-side wiring branch TDO which respectively branch off from an input-side end portion 18 and an output-side end portion 34 of said boundary scan test circuit 16 are formed; and said input-side wiring branch TDI is for inputting test data from outside (via module test data input MTDI, note column 6 lines 35-37) and said output-side wiring branch TDO is for outputting a test result directly to outside (via MTDO, note column 6 lines 41-43), wherein a scan-in terminal 36 through which an internal scan test signal is input is connected to said input-side wiring branch TDI; wherein a scan-out terminal 38 through which a scan test result is output is connected to said output-side wiring branch TDO; and wherein an input to said in-chip chain can be selected (via register 20) from a signal in said boundary scan test circuit 16 and a signal from said wiring branch. Note figures 3-6 and 9-12 of Jarwala et al.

Jarwala et al. do not disclose that said ceramic is semiconductor material. However, Komoike discloses a semiconductor wiring substrate 1 being composed of a semiconductor (note figure 1) on which a plurality of semiconductor chip IPs 2,4 are to be mounted; and a plurality of pieces of wiring 7 formed on the semiconductor substrate 1 to be used only for testing. Note figure 1 of Komoike. Why should one substitute the semiconductor substrate of Komoike for the ceramic substrate of Jarwala et al.? One having skill in the Multi-chip Module Art would know. A mismatch in the materials used

Art Unit: 2826

for the substrate and the chips bonded thereon could result in a TCE (thermal coefficient of expansion) mismatch. When the assembly is heated, the substrate and chips could expand at different rates, resulting in potentially damaging stress between the constituent parts. This problem is often discussed in the art, for example at column 1 lines 17-40 of Canestaro et al. 4,728,751. Therefore, it would have been obvious to a person having skill in the art to replace the ceramic material of Jarwala et al.'s substrate with the semiconductor material such as taught by Komoike in order to match the material, and thus the CTE, of the chip IPs to thus avoid possible damage due to thermal stress.

#### ***Allowable Subject Matter***

4. Claims 13 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

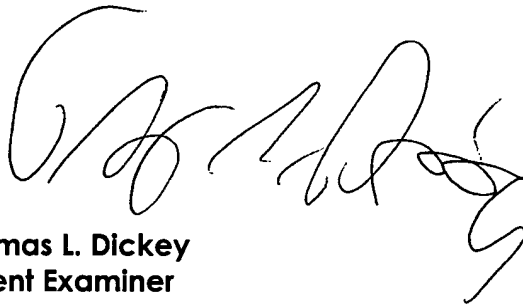
#### ***Conclusion***

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2826

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Thomas L. Dickey', is written over the printed name and title.

**Thomas L. Dickey**  
**Patent Examiner**  
**Art Unit 2826**  
**06/06**